REMARKS

Summary of the Office Action

Claims 1, 2, and 5 stand objected to.

Claims 5-11, 15, and 16 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claim 15 stands rejected under 35 U.S.C. § 112, second paragraph, as failing to conform to U.S. practice.

Claims 1, 3, and 4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Watt* (U.S. Patent No. 5,623,156) in view of *Yu* (U.S. Patent No. 5,361,185).

Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Watt*, in view of *Yu*, and further in view of *Ker* (U.S. Patent No. 6,075,686).

Claims 5-11, 15, and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Watt*, in view of *Yu*, and further in view of *Staab* (U.S. Patent No. 5,610,790).

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Watt*, in view of *Yu*, and further in view of *Staab* and *Ker*.

Summary of Response to Office Action

By this amendment, Applicant amends claims 1, 2, 5, 7, 10, and 15 in order to clarify the claimed invention and to expedite the prosecution of this application.

All Claims Define Allowable Subject Matter

Applicant respectfully submits that claims 1, 2, and 5 have been amended to comply with the Examiner's objections. Applicant submits that the misspelling of the word "difference" was corrected by a Preliminary Amendment, filed September 13, 2000, whereby Applicant amended claims 1 and 5 by substituting the word "different." Applicant respectfully requests the Examiner to withdraw the objections to the claims.

Applicant also submits that the specification has been amended to comply with Examiner's objections. Thus, the Applicant respectfully requests the Examiner withdraw his objections to the specification.

Claims 5-11, 15 and 16 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 15 stands rejected under 35 U.S.C. § 112, second paragraph, as failing to conform to current U.S. practice. The rejections are respectfully traversed.

The Office Action states that it is unclear if "said active element" recited in line 20 of claim 5 is associated with the first or second connection configuration. Applicant submitted a Preliminary Amendment on September 13, 2000, amending claim 5 by inserting the phrase "in a second connection configuration" before the word "being" in line 20.

Applicant respectfully submits that claims 5-11, 15, and 16 fully comply with the requirements of 35 U.S.C. § 112. Accordingly, Applicant respectfully submits that the rejections under 35 U.S.C. § 112, second paragraph, should be withdrawn.

With respect to the rejection of independent claim 1 under 35 U.S.C. § 103(a) as being obvious over *Watt* in view of *Yu*, Applicant respectfully traverses the rejection for at least the reason that the rejection fails to set forth a *prima facie* case of obviousness. The Office bears the initial burden of establishing a *prima facie* case of obviousness. MPEP § 2142. If the Office fails to set forth a *prima facie* case of obviousness, Applicant is under "no obligation to submit evidence of nonobviousness," such as unexpected results or commercial success. *Id.* In other words, if the Office fails to meet the initial burden of establishing a *prima facie* case of obviousness as to a given claim, then that claim is not obvious without any evidence of nonobviousness by Applicant.

In order to establish a *prima facie* case of obviousness, the Office must satisfy three requirements. MPEP § 2142. First, "the prior art reference, or references when combined, must teach all the claim limitations." *Id.* Second, the Office must show that there is "some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." *Id.* Finally, "there must be a reasonable expectation of success." *Id.*

At the outset, it is respectfully submitted that none of the applied art discloses or teaches at least the feature of "said inter-circuit signal wire is not directly connected to an input circuit or an output circuit." *Watt* (Figures 5, 8) discloses that the inter-circuit signal wire connecting the input buffer 12 and ouput buffer 14 is also connected to I/O pad 16. Also, *Yu* (Figure 1) shows the inter-circuit signal wire directly connecting the pad 14 to the ESD structure 12 and internal circuit 16. Accordingly, the Applicant respectfully requests the Examiner to withdraw the rejection of claim 1 because the combination of *Watt* in view of *Yu* fails to teach or suggest the claimed invention as a whole.

Moreover, the Office Action fails to show that one of ordinary skill in the art would have reasonably expected success by modifying *Watt* in view *Yu* as suggested by the Office Action. Applicant teaches that "basic semiconductor parts are generalized and utilized in common, and a variety of circuits are implemented by changing the allocation of active elements" to provide resistance to electrostatic breakdown. (Specification at page 10, lines 7-9.) Active elements in the second connection configuration that are used as protection elements and that have similar or identical structure to the active element in the first connection configuration make it possible to realize a semiconductor integrated circuit device which is resistant to electrostatic breakdown and suitable to automatic designing.

On the other hand, *Watt* discloses at col. 5, lines 63-64 a primary ESD protection circuit 18 and a secondary ESD protection circuit 20 for providing ESD protection. The primary circuit 18 includes stacked diodes D_1 and D_2, and the use of such a setup is "well known and conventional in the art." (*Watt*, col. 6, lines 2-5) In addition, the secondary circuit 20 uses a transistor M_0 in conjunction with a resistor R. (*Watt*, Fig. 5).

The Office Action suggests at page 4, lines 18-21, that the M_0 is the active element in the second connection configuration. This would require the secondary ESD protection circuit 20 to serve as the second connection configuration in the present invention. However, *Watt* discloses the amount of charge that flows through the secondary ESD protection circuit 20 is relatively small in relation to the primary ESD protection circuit 18. As a result, a person having ordinary skill in the art reading *Watt* in view of *Yu*, would still use conventional inter-block protection circuits, such as the stacked diode circuit in *Watt*, to provide sufficient ESD protection.

Furthermore, the combination of *Watt* in view of *Yu* fails to teach or suggest at least the feature of "a plurality of internal circuits arranged internally in a circuit forming region." *Watt*

discloses a single internal circuit 12. *Yu* also discloses a single internal circuit 18. Thus, the combination of *Watt* in view of *Yu* fails to set forth a *prima facie* case of obviousness as the combination of references fails teach or suggest all the features of the claimed invention.

Moreover, the combination of *Watt* in view of *Yu* fails to teach or suggest at least the feature of "said plurality of active elements in said second connection configuration being arranged adjacent to said active element in the first connection configuration to sandwich or surround said active element in the first connection configuration." The Office Action at page 5, lines 5-10 states that *Yu* teaches that the active elements of a first and another configurations must be placed in close proximity.

Yu (Figure 2) discloses an ESD structure 12 comprising a plurality of transistors Q1-Q3 and a clamp 10 located in close proximity to internal circuit 16. However, neither the ESD structure 12 nor clamp 10 sandwich or surround the internal circuit 16 as recited in claim 1. As a result, the combination of *Watt* in view of *Yu* fails teach or suggest the claimed invention as a whole.

Further, since claims 2-4 depend from and respectively incorporate all the features of independent claim 1, dependent claims 2-4 are not obvious for at least the reasons for which claim 1 is not obvious. Thus, Applicant respectfully request that the rejection of dependent claims 2-4 under 35 U.S.C. § 103(a) be withdrawn.

With respect to the rejection of independent claim 5 under 35 U.S.C. § 103(a) as unpatentable over *Watt*, in view of *Yu,* and further in view of *Staab*, Applicant respectfully traverses the rejection because the Office Action fails to put forth a *prima facie* case of obviousness.

Applicant respectfully submits that none the applied art discloses or teaches at least the feature of "said inter-circuit signal wire is not directly connected to an input circuit or an output circuit." *Watt* (Figures 5, 8) discloses that the inter-circuit signal wire connecting the input buffer 12 and ouput buffer 14 is also connected to I/O pad 16. Next, *Yu* (Figure 1) shows the inter-circuit signal wire directly connecting the pad 14 to the ESD structure 12 and internal circuit 16. Finally, *Staab* (Figure 7) illustrates that the inter-circuit signal wire connects input pad 701 directly to the ESD protection circuit 700 at node 715, which is further connected to protected circuit 711. Accordingly, the Applicant respectfully requests the Examiner to withdraw the rejection of claim 5 because the combination of *Watt* in view of *Yu*, and further in view of Staab, fails to teach or suggest the claimed invention as a whole.

Moreover, the Office Action fails to show that one of ordinary skill in the art would have reasonably expected success by modifying *Watt* in view *Yu,* and further in view of *Staab* as suggested by the Office Action. According to the Office Action at page 8, lines 6-8, *Staab* discloses a cross power supply clamp 716 with a similar structure to the active element (element 12 in Fig. 5 of *Watt*) in the first connection configuration. However, *Staab* still requires that diodes 702 and 703 be used in conjunction with cross power supply claim 716 to provide sufficient ESD protection. Consequently, one having ordinary skill in the art would still use conventional inter-block protection circuits, such as the diode arrangement in *Staab*, to provide sufficient ESD protection. Thus, Applicant respectfully requests the Examiner to withdraw the rejection of claim 5 under 35 U.S.C § 103(a), because the combination of references cited by the Office Action fails to teach or suggest the claimed invention as a whole.

Furthermore, the combination of *Watt* in view of *Yu* fails to teach or suggest at least the feature of "a plurality of internal circuits arranged internally in a circuit forming region." *Watt*

discloses a single internal circuit 12. *Yu* also discloses a single internal circuit 18. *Staab* discloses a single protected circuit 711. Thus, the combination of *Watt,* in view of *Yu* and *Staab*, fails to set forth a *prima facie* case of obviousness as the combination of references fails teach or suggest all the features of the claimed invention.

Further, since claims 6-11, 15, and 16 depend from and respectively incorporate all the features of independent claim 5, dependent claims 6-11, 15, and 16 are not obvious for at least the reasons for which claim 5 is not obvious. Thus, Applicants respectfully request that the rejection of dependent claims 6-11, 15, and 16 under 35 U.S.C. § 103(a) also be withdrawn.

CONCLUSION

With no other rejection pending, Applicant respectfully submits that claims 1-11, 15, and 16 are allowable. Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicant's undersigned representative to expedite prosecution.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attachment is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

DATE: January 30, 2003

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT:

Please amend the abstract as follows:

A semiconductor integrated circuit device having a plurality of internal circuits connected to different power lines, and an inter-circuit signal wire or a branched wire along these internal circuits, wherein near an active element in a first connection configuration connected to the inter-circuit signal wire or the like, a plurality of active elements in a second [another]connection configuration are arranged to sandwich or surround the active element in the first connection configuration. The active elements in the second [another] connection configuration have the identical or similar structure to the active element in the first connection configuration, and are connected to power lines of an internal circuit associated therewith but not connected to signal wires and so on in the internal circuit.

IN THE SPECIFICATION:

Please amend the specification as follows:

On page 6, line 13 please substitute the following paragraph:

Further, as can be seen in Fig. 10B, for [For] communicating signals between the internal circuits 4A, 4B, inter-circuit signal wires 12 for interconnecting the output element 12A of the internal circuit 4A and the input [output] element 12B of the internal circuit 4B, and inter-circuit signal wires 13 for interconnecting the output element 13B of the internal circuit 4B and the input element 13A of the internal circuit 4A are also routed between the internal circuits 4A, 4B as many number of lines as required for communicating signals.

On page 6, line 21 please substitute the following paragraph:

The output element 12A may comprise a single or a plurality of active elements such as transistors. For example, if the output element 12A is a CMOS invertor (see Fig. 11A), the output element 12A includes a p-type MOS (hereinafter called the "pMOS") transistor 12AP having a source connected to the power line 8A, a drain connected to the inter-circuit signal wire 12, and a gate connected to an internal signal wire SA within the internal circuit 4A; and an n-type MOS (hereinafter called the "nMOS") transistor 12AN having a source connected to the power line 9A, a drain connected to the inter-circuit signal wire 12, and a gate connected to the internal signal wire SA within the internal circuit 4A. The input element 12B also includes a pair of transistors, pMOS transistor 12BP and nMOS transistor 12BN, having their sources connected to the power lines 8B, 9B, respectively, which have their gates connected to the inter-circuit signal wire 12, and their drains connected to an internal signal wire SB within the internal circuit 4B.

On page 7, line 11 please substitute the following paragraph:

The input element 13A and the output element 13B, though signals are communicated in directions opposite to each other, each includes [include] a similar transistor pair consisting of one pMOS transistor (13AP, 13BP [13AN]) and one nMOS transistor [pair] (13AN [13BP], 13BN), with their drains or gates connected to the inter-circuit signal wire 13.

On page 9, line 11, please substitute the following paragraph:

Specifically, as can be seen in Fig. 11D, basic cells of interest are formed with contact holes (see a black line [circuit] in Fig. 11D) such as via holes at the centers thereof to connect the sources of the active elements 12AP, 12AN, 12BP, 12BN in the first connection configuration to

the power lines 8A, 9A, 8B, 9B, respectively. In the internal circuit 4A, the internal signal wire SA is connected to the gate of the active element 12AP in the first connection configuration as well as to the gates of both the active elements 12AP, 12AN in the first connection configuration. Also, one end of the inter-circuit signal wire 12 is branched and connected to the drains of the active elements 12AP, 12AN in the first configuration at corners of the basic cells.

On page 12, line 6, please substitute the following paragraph:

Also, in such a situation, if surge noise is introduced, for example, into the input/output terminal 7B (see Fig. 12C), the existence of the input protection circuit 3B for protecting the internal element 11B may adversely affect the other internal element 12B and so on. The surge noise will be forced to escape to the power lines 8B, 9B through the input protection circuit 3BB, and then is discharged to the outside from the lower power terminal 5B and the ground terminal 6B, and also propagates and diffuses across the internal circuit 4B. In this event (see two-dot chain lines and so on in Fig. 12C), the difference between a time required for the surge noise to reach the active element 12BP in the first connection configuration through the power line 8B and a time required for the surge noise to reach the active element 12BN in the first connection configuration through the power line 9B cannot be ignored. In addition, it is also contemplated that an element which has <u>been</u> intensively and locally affected by the difference in potential with the inter-circuit signal wire 12 has <u>also</u> become more susceptible to failure.

<u>IN THE CLAIMS:</u>

Please amend the claims as follows:

1. (Amended Twice) A semiconductor integrated circuit device comprising:

a plurality of internal circuits arranged internally in a circuit forming region, said internal circuits having different power lines;

an inter-circuit signal wire arranged to interconnect said internal circuits, wherein said inter-circuit signal wire is not directly connected to an input circuit or an output circuit; and

a plurality of active elements in a second [another] connection configuration including

elements of an identical or similar structure to an active element in a first connection configuration connected to said inter-circuit signal wire,

said plurality of active elements in said second connection configuration being arranged adjacent to [near] said active element in the first connection configuration to sandwich or surround said active element in the first connection configuration,

said plurality of active elements in said second [another] connection configuration being connected to power lines of said internal circuits associated therewith and being isolated from signal wires other than said inter-circuit signal wire.

2. (Amended Twice) A semiconductor integrated circuit device according to claim 1, wherein each of said internal circuits includes a plurality [multiplicity] of basic cells [for active elements] regularly arranged in repetition, and said active element in the first connection configuration and said plurality of active elements in the second [another] connection configuration are allocated to some of said basic cells.

5. (Amended Twice) A semiconductor integrated circuit device comprising:

a plurality of internal circuits arranged internally in a circuit forming region, said internal circuits having different power lines;

an inter-circuit signal wire arranged to interconnect said internal circuits, wherein said inter-circuit signal wire is not directly connected to an input circuit or an output circuit; and

an active element in a second connection configuration arranged adjacent to [near] an active element in a first connection configuration connected to said inter-circuit signal wire, including

an element of an identical or similar structure to said active element in the first connection configuration,

said active element in a second connection configuration being connected to power lines of said internal circuits associated therewith and being isolated from said inter-circuit signal wire and other signal wires.

7. (Amended) A semiconductor integrated circuit device according to claim 5, wherein each of said internal circuits includes a plurality [multiplicity] of basic cells [for active elements] regularly arranged in repetition, and said active element in the first connection configuration and said plurality of active elements in the second connection configuration are allocated to some of said basic cells.

10. (Amended Twice) A semiconductor integrated circuit device according to claim 5, further comprising an active element in a third connection configuration, arranged adjacent to [near] said active element in the first connection configuration and including an element of an identical or similar structure to said active element in the first connection configuration, said active element in the third connection configuration being connected to a power line of an internal circuit associated therewith and said inter-circuit signal wire and being isolated from other signal lines.

15. (Amended Twice) A semiconductor integrated circuit device according to claim 10, wherein:

a plurality of said inter-circuit signal wires having different communication directions from each other are arranged to interconnect a pair of internal circuits;

said active element in the second connection configuration and said active element in the third connection configuration are arranged adjacent to [near] said active element in the first connection configuration on a reception side of said inter-circuit signal wire in one of said pair of internal circuits; and

said active elements in the third connection configuration are arranged independent [instead of or exclusive] of said active element in the second connection configuration, near said active element in the first connection configuration on a reception side of said inter-circuit signal wire in the other one of said pair of internal circuits.